Status of Off-Detector Electronics
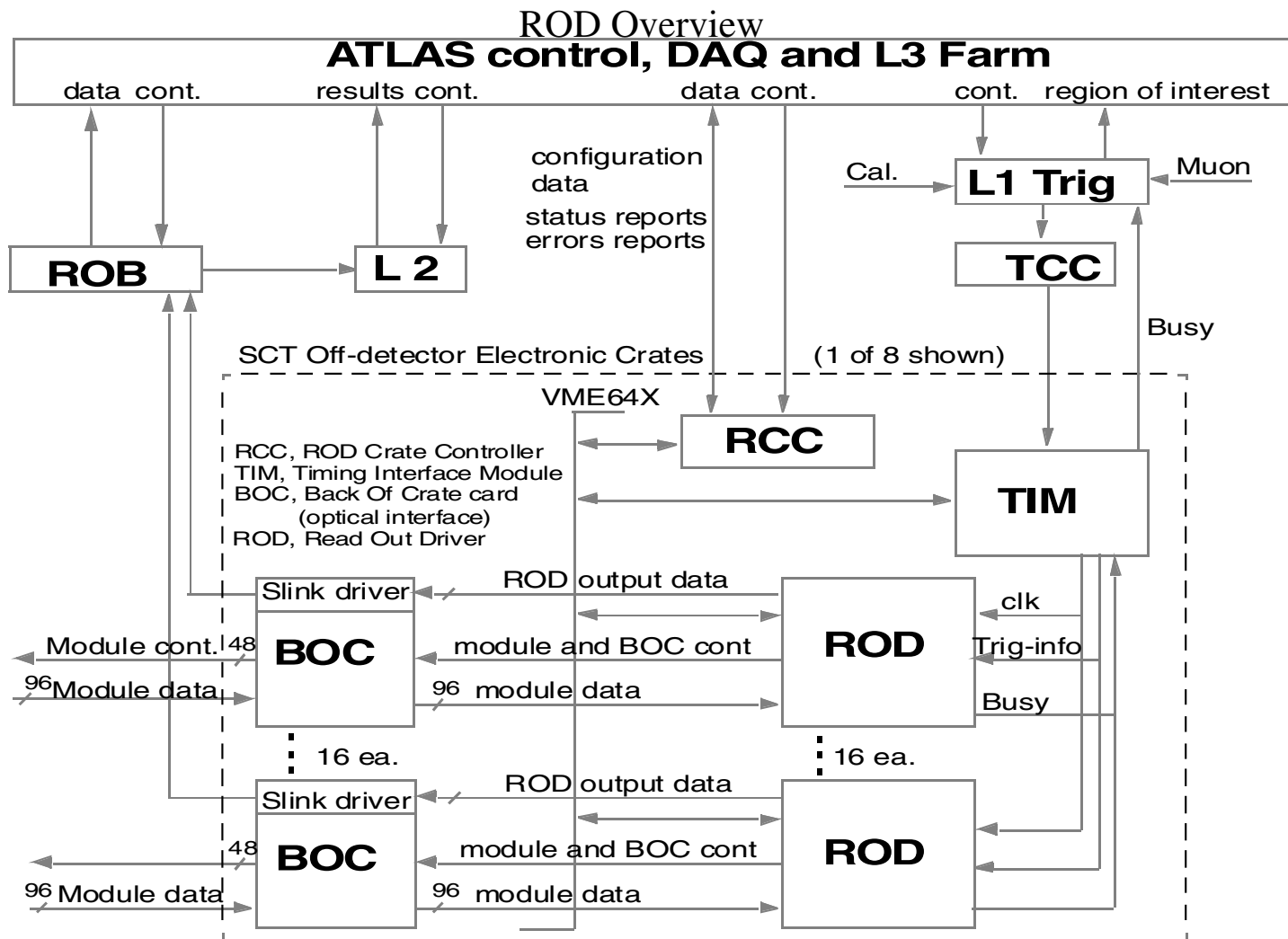
K. Einsweiler, LBNL

System consists of ROD, TIM, ROD Crate Backplane, and BOC (Back of Crate Optocard).

- ROD is joint LBL/Wisconsin development (Jared)

- TIM is a UCL Development (Lane)

- Backplane is an Oxford/RAL development (Wastie)

- BOC is a Cambridge development (Goodrick)

- First prototypes now fabricated and undergoing lab testing.

- Emphasis for first tests is on SCT version, but pixel version involves (in principle) only firmware changes.

- Further information on all components:
  http://www-wisconsin.cern.ch/~atlas/off-detector/off-detector.html

System Block Diagram

Reminder of what the blocks are:

- ROD Crate includes 16 (ROD+BOC) cards (two groups of 8, with TIM in center), one TIM, and one RCC, sitting in a 9U VME64x crate with a custom backplane.

ROD Overview

ATLAS control, DAQ and L3 Farm

data cont.   results cont.   data cont.   cont.   region of interest

configuration data

Cal. → **L1 Trig** ← Muon

status reports
errors reports

ROB → **L 2**

TCC

Busy

SCT Off-detector Electronic Crates   (1 of 8 shown)

VME64X

RCC

RCC, ROD Crate Controller
TIM, Timing Interface Module
BOC, Back Of Crate card
    (optical interface)
ROD, Read Out Driver

TIM

Slink driver ← ROD output data

Module cont. 48 **BOC**   module and BOC cont   **ROD**   Trig-info

96 Module data   96 module data   Busy

clk

16 ea.   16 ea.

Slink driver ← ROD output data

48 **BOC**   module and BOC cont   **ROD**

96 Module data   96 module data

2

Status of ROD Prototype

## Program for prototyping (Joseph, Nagel, Holmes):

- Initial fabrication run of three boards completed.

- One board partially loaded. Control path is fully loaded, external interface circuitry loaded, but data path is only a "slice" including 2 formatter FPGAs, one Fragment Builder FPGA, one Router FPGA and one Backend DSP.

- This board is presently being tested:
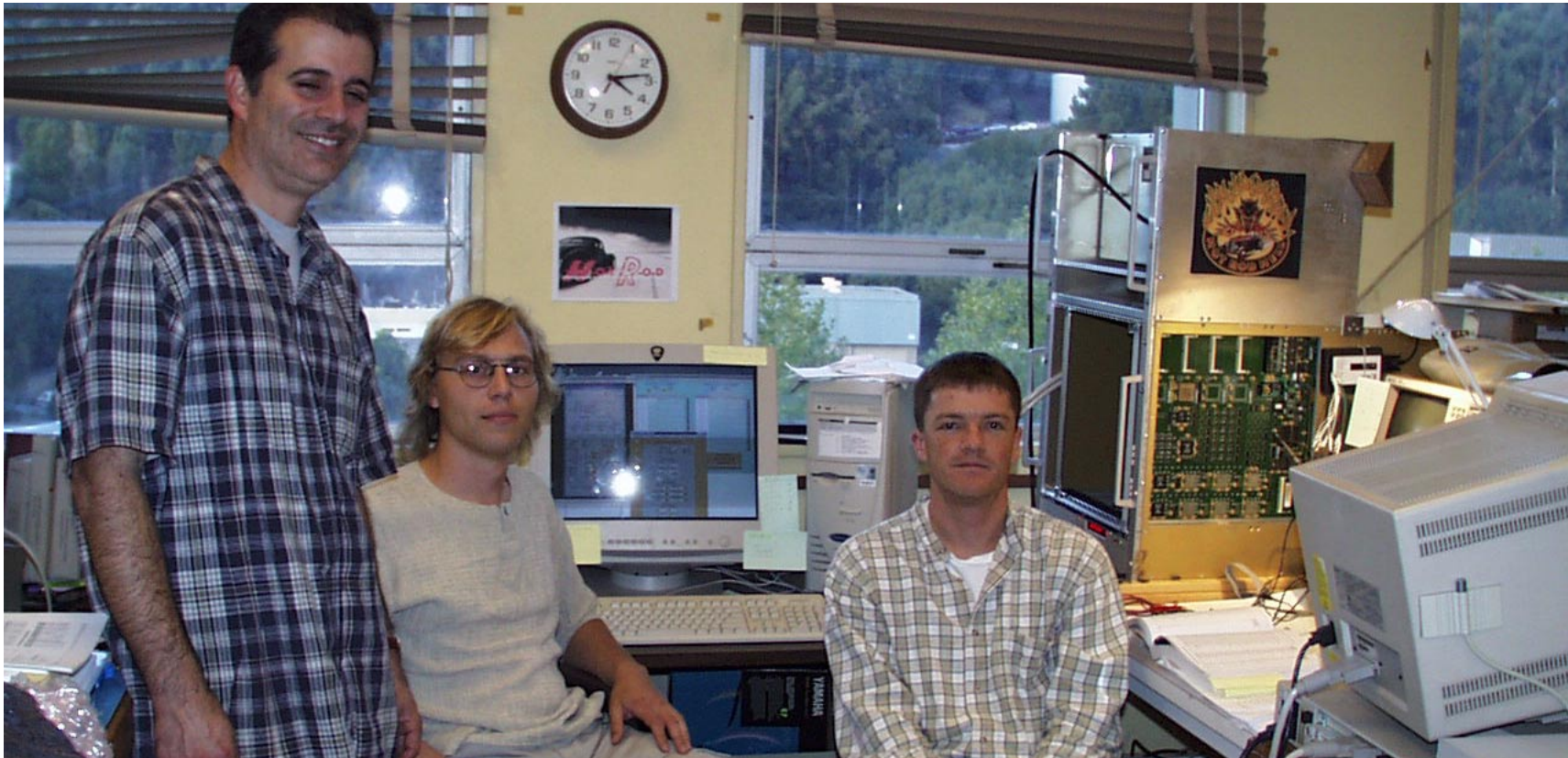
•Top level schematic:
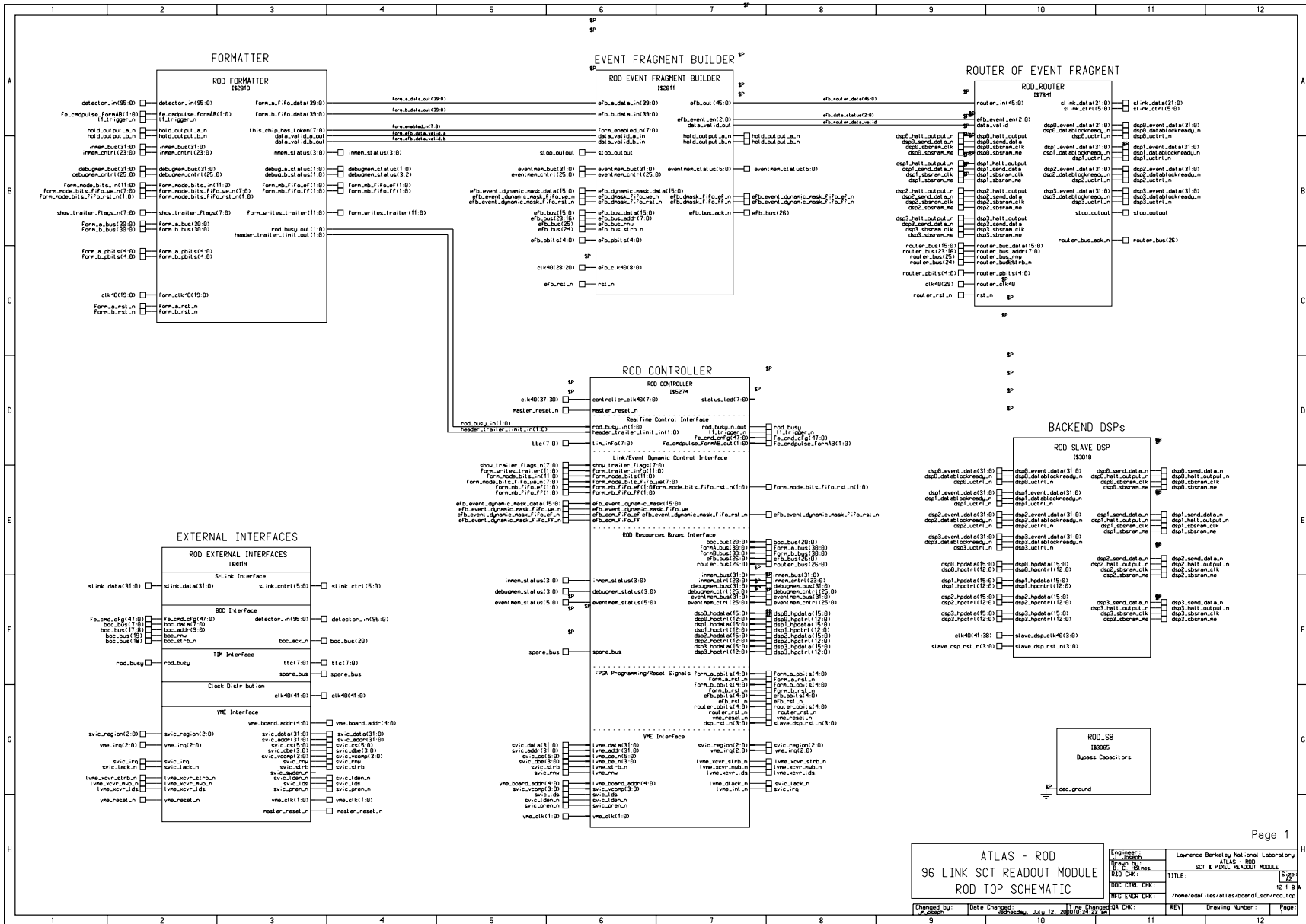
- Partial loading of board:
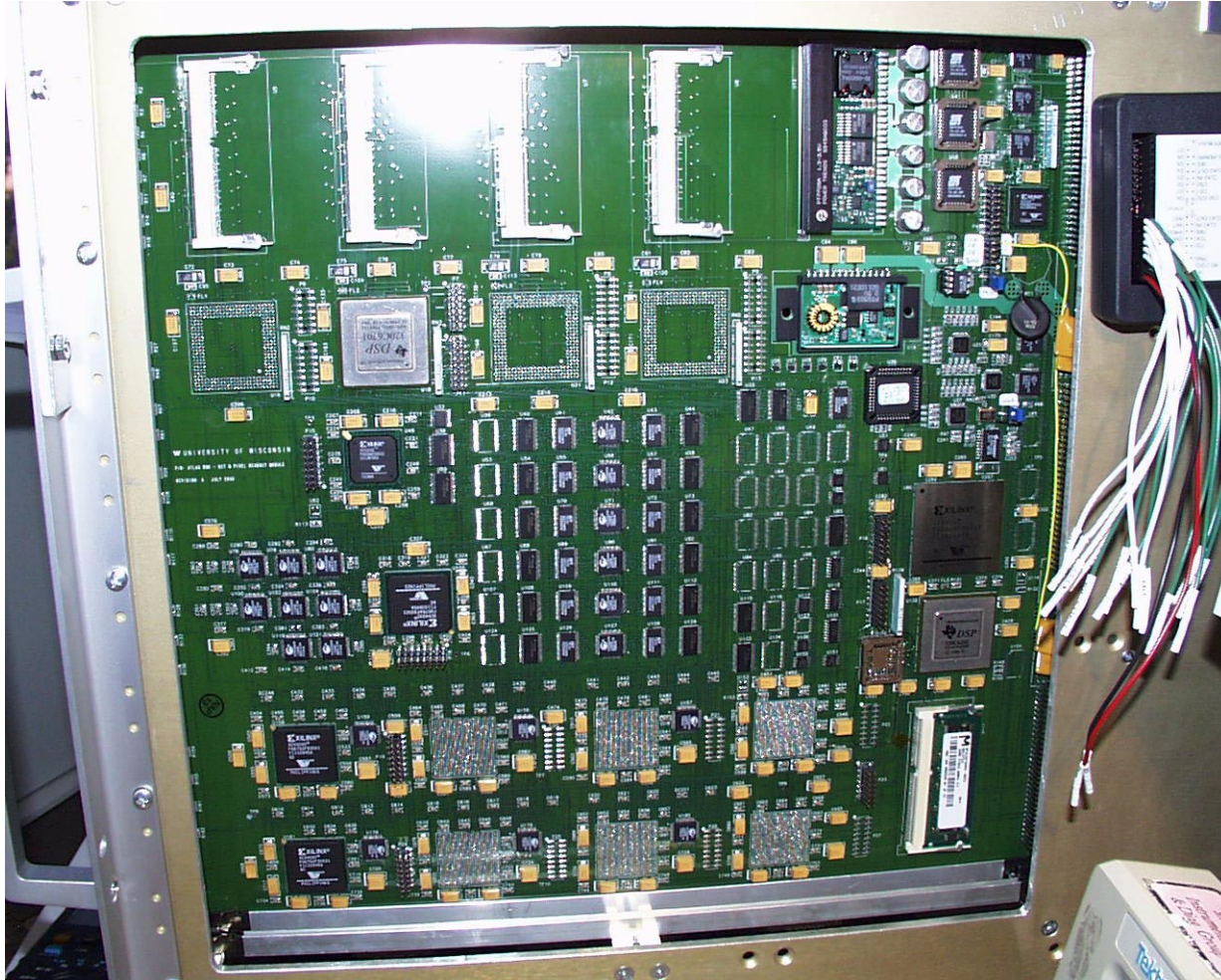
- All blocks in control path and external interface were loaded. This includes VME interface, Program and Reset Manager FPGA, ROD Resources and Interface FPGA (RRIF), Master DSP, BOC and TIM interfaces and S-link interface.

- Several minor problems found, but board is beginning to operate in a useful way.

Summary of status:

- VME interface is working, except for a small protocol problem for data transfers between VME and DSP which needs additional logic for one signal.

- Program Manager FPGA, which controls initialization and reconfiguration of all FPGAs and DSPs on ROD from Flash memories, is basically working.

- Master DSP, which is connected to VME via its Host Port Interface, and provides most of the intelligence in the ROD controller, is now alive and able to execute instructions loaded from host PC.

- Resources and Interface FPGA, which controls access to all internal blocks of the ROD via extensive transceiver paths, just beginning to be debugged.

- Conclude: Control paths are close to being functional.

Next steps:

- Use loop-back boards and special software to allow datapath testing. This relies on internal memories to act as data sources and sinks, and RRIF ability to modify paths between different blocks to allow exercising single blocks.

- Once datapath tests are OK, bring ROD to Cambridge and integrate with TIM, BOC, and crate backplane, to make sure that all communication is working.

- Revise boards to include all schematic updates, and fabricate 10 of the revised boards. Debug them and circulate them to the SCT and Pixel user communities.

ROD DSP Software Status (Damon):

- •Master DSP code to provide environment is complete.

- •This includes the ability of the Master DSP to process primitive lists from the host (RCC), and return data, status, and error information.

- •Specific primitives have been written to allow reading/writing of all internal ROD registers and memories, as well as configuring of the Slave DSPs.

ROD Test Stand Software Status (Lukas):

- •Basic software framework is written using LabWindows and PC. Many aspects of this would be included in basic libraries which would be used on the RCC to build more complex applications.

- •Support provided now for VME read/write, Master DSP read/write, Flash memory read/write, and Status Register read/write.

- •Next layer of software includes List Formatter for primitive lists to send to Master DSP, Host Control for Master DSP to initialize and configure, and Reply Processor to handle returned data from ROD.

ROD DAQ Support (Tom Meyer):

- •Design and implementation of DAQ-related primitives, including many aspects of Slave DSP operation.

TIM Status:

- Two prototype boards built and under test at UCL.

- VME access to all registers working. Clock and sequencer signals get through to the backplane.

- TTC system to provide input to TIM is working.

- Testing of stand-alone operation and many details of internal logic not yet completely programmed and/or tested.

BOC Status:

- Partially loaded BOC card under test in Cambridge. Control of basic settings is operational (delays, etc).

- Delays in obtaining DRX/BPM opto-interfaces chips, and VCSEL and PIN arrays.

- Also presently loading VME test board to allow stand-alone access to BOC bus.

Backplane Status:

- First two backplanes fabricated and delivered to Oxford, now being assembled

System Integration:

- Indications are that the ingredients are almost there for moving to the integration and test period in Cambridge in Jan-Mar 2001.

Plans for Pixel Evaluation:

- Clearly, SCT will lead the way in the evaluation, including initial system testing in Cambridge early next year, and operation in system test facility at CERN in the first half of 2001.

- John Richardson will work with LabWindows test environment created by Lukas at LBL, and add some of the PixelDAQ functionality. This should allow us to operate a ROD in a lab-test environment, with some of the PLL capabilities that we are used to, for example doing threshold/timewalk/TOT scans of modules.

- We would plan to perform initial evaluations of the ROD in the lab using existing modules and direct connection to the BOC connector (a "poor-mans BOC" with copper links for a few modules). The goal would be to use the 3-module disk sector that we plan to construct from Flex2/FE-B modules as the device to test. This would allow us to carry out useful tests during the ROD evaluation period.

- The next step should involve a more complete system test, including realistic pigtails, a PP0 cable with an opto-daughter card with six parallel links, and a real service bundle for a half-stave and/or a sector. This would probably be delayed until we can build FE-I modules, but everything else should be carefully prepared in advance so that we could proceed rapidly when new modules are ready.

More planning, manpower, and modules required for next steps in ROD evaluation and system testing!